In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Original) An apparatus for use in a computer graphics system, comprising:

a plurality of depth buffers for storing depth data, wherein at least one of the plurality of depth buffers is configured to provide depth data for a group of pixels, wherein at least one other of the plurality of depth buffers is configured to provide depth data for each pixel of the group;

a plurality of stencil buffers, the stencil buffers configured to store stencil shadow volume data, wherein at least one of the plurality of stencil buffers is configured to provide stencil shadow volume data for the group of pixels; wherein at least one other of the plurality of stencil buffers is configured to store stencil shadow volume data for each pixel of the group; and

control logic for controlling the plurality of stencil buffers and the plurality of depth buffers, wherein the stencil shadow volume data is generated and stored.

2. (Original) The apparatus of claim 1, wherein the plurality of depth buffers comprise:

a first depth buffer, wherein the first depth buffer has a plurality of first depth buffer records, such that each first depth buffer record stores depth data for a group of pixels, where the group of pixels comprises a tile; and

a second depth buffer, wherein the second depth buffer has a plurality of second depth buffer records, wherein each second depth buffer record stores depth data for a pixel.

3. (Original) The apparatus of claim 2, wherein the plurality of the stencil buffers comprise:

a first stencil buffer, wherein the first stencil buffer has a plurality of first stencil buffer records, such that each first stencil buffer record stores the stencil shadow volume data for the tile; and

a second stencil buffer having a plurality of second stencil buffer records, such that each second stencil buffer record stores the stencil shadow volume data for each pixel, wherein the second stencil buffer record is configured as a partition of the second depth buffer record.

4. (Original) The apparatus of claim 3, further comprising:

a first cache, wherein the first cache is configured to communicate data with the first depth buffer; wherein the first cache is further configured to communicate data with the first stencil buffer; and

a second cache, wherein the second cache is configured to communicate data with the second depth buffer, wherein the second cache is further configured to communicate data with the second stencil buffer.

5. (Currently amended) The apparatus of claim 4, further comprising a plurality of subtiles, wherein each tile is divided into a plurality of subtiles, wherein the stencil shadow volume data stored in the first stencil buffer record comprises:

a reference value for each of the plurality of subtiles;

a delta value for each pixel comprised in the group of pixels; and

a plurality of subtile status flags.

6. (Original) The apparatus of claim 5, further comprising a FIFO hardware structure, wherein the FIFO hardware structure is configured to store the first stencil buffer record.

7. (Original) The apparatus of claim 5, wherein the plurality of subtile status flags comprise a plurality of subtile dirty flags, a plurality of subtile overflow flags and a plurality of subtile underflow flags, wherein there is one of the plurality of subtile dirty flags corresponding to each one of the plurality of subtiles; wherein there is one of the plurality of subtile overflow flags corresponding to each one of the plurality of subtiles; wherein there is one of the plurality of subtile underflow flags corresponding to each one of the plurality of subtiles.

8. (Original) The apparatus of claim 4, wherein the plurality of stencil buffers resides within any of a plurality of hardware memory structures.

9. (Original) The apparatus of claim 4, wherein the plurality of depth buffers resides within any of a plurality of hardware memory structures.

10. (Original) The apparatus of claim 4, wherein the plurality of data caches is located on a computer graphics processor.

11. (Currently amended) A method for generating a shadow effect in a computer graphics system, comprising the steps of:

rendering an object with diffuse color;

generating pixel depth information for a scene for storage in a pixel depth buffer;

generating depth information for a group of pixels, wherein the depth information for the group of ~~pixel~~ pixels is stored in a compressed depth buffer;

testing the depth information in the compressed depth buffer to determine if the group of ~~pixel~~ pixels may utilize a shadow mask data in a compressed stencil buffer;

generating the shadow mask data; wherein a first portion of the shadow mask data is generated in the compressed stencil buffer, wherein a second portion of the shadow mask data is generated in a pixel stencil buffer;

generating a shadow area, wherein the shadow area is determined by the shadow mask data contained in the compressed stencil buffer and the pixel stencil buffer; and

adding specular color to objects not in the shadow area.

12. (Original) The method of claim 11, further comprising the step of:

generating a shadow volume, wherein the shadow volume comprises a plurality of front-facing polygons relative to a viewpoint, wherein the shadow volume further comprises a plurality of back-facing polygons relative to the viewpoint.

13. (Original) The method of claim 12, further comprising the step of selectively incrementing a subtile reference value.

14. (Original) The method of claim 13, further comprising the step of selectively decrementing the subtile reference value.

15. (Original) The method of claim 14, wherein the group of pixels is a tile.

16. (Original) The method of claim 14, wherein the group of pixels is a subtile.

17. (Currently amended) The method of claim 14, further comprising the step of setting a plurality of status flags in the compressed stencil buffer, wherein the plurality of status flags are set to indicate that a portion of the shadow mask data in the compressed stencil buffer is incomplete.

18. (Original) The method of claim 17, further comprising the step of selectively merging the shadow mask data in the compressed stencil buffer into the pixel stencil buffer; wherein the states of the plurality of status flags are utilized to select which shadow mask data from the compressed stencil buffer is merged into the pixel stencil buffer.

19. (Original) A computer graphics system comprising:

depth data compression logic configured to generate a compressed depth data, where the compressed depth data corresponds to a group of pixels;

shadow data compression logic configured to generate a compressed stencil shadow data, where the compressed stencil shadow data corresponds to the group of pixels, wherein the compressed stencil shadow data is generated utilizing a stencil shadow volume method;

shadow data generation logic configured to generate an uncompressed stencil shadow data, wherein the uncompressed stencil shadow data is generated utilizing the stencil shadow volume method; and

shadow data merging logic configured to selectively merge the compressed stencil shadow data with the uncompressed stencil shadow volume data.

20. (Original) The shadow data generation logic of claim 19, further configured to selectively generate the uncompressed stencil shadow data, wherein the uncompressed data is selectively generated based on the compressed stencil shadow data exceeding a range, wherein the range is determined by a format of the compressed stencil shadow data.

21. (Original) The shadow data merging logic of claim 20, further configured to selectively merge the compressed stencil shadow data and the uncompressed stencil shadow data, wherein the merge operation is determined by the state of a plurality of data status flags.

22. (Original) The shadow data merging logic of claim 21, wherein one of the plurality of data status flags comprises a subtile underflow flag.

23. (Original) The shadow data merging logic of claim 21, wherein one of the plurality of data status flags comprises a subtile overflow flag.

24. (Original) The shadow data merging logic of claim 21, wherein one of the plurality of data status flags comprises a subtile dirty flag.

25. (Original) Computer graphics hardware, comprising a means for creating a shadow effect using a compressed stencil buffer.

26. (Original) The computer graphics hardware of claim 25, further comprising:

means for selectively merging shadow mask data for a tile into a pixel stencil buffer, wherein the tile corresponds to a record in the compressed stencil buffer; wherein the tile is comprised of a group of pixels; wherein a subtile is comprised of a subset of the group of pixels.

27. (Original) The computer graphics hardware of claim 26, further comprising:

means for storing a pixel depth data in a pixel depth data buffer; and

means for storing a compressed depth data in a compressed depth data buffer, wherein the compressed depth data corresponds to the tile.

28. (Original) The computer graphics hardware of claim 27, further comprising a means for determining which pixels are in a shadow.

29. (Original) The computer graphics hardware of claim 28, wherein the means for determining which pixels are in a shadow comprises selectively performing a depth data test on compressed depth data and pixel depth data, wherein the means for determining which pixels are

in a shadow further comprises selectively performing a stencil value not equal to zero test on pixel stencil data and compressed stencil data.

30. (Original) The computer graphics hardware of claim 29, further comprising a means for adding specular color to pixels not contained in the shadow.